LIQUID CRYSTAL DISPLAY APPARATUS WITH ADDRESS MARKS CONNECTED TO CONNECTIONS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display (LCD) apparatus, and more particularly, to the improvement of address marks for easily specifying a defective location in the LCD apparatus.

Description of the Related Art

Generally, a prior art LCD apparatus is constructed by a transparent substrate, a plurality of gate bus lines formed on the transparent substrate, a plurality of signal bus lines formed on the transparent substrate substantially perpendicular to the gate bus lines, a plurality of common electrode lines formed on the transparent substrate in parallel with the gate bus lines, and a plurality of pixels connected to one of the gate bus lines, one of the signal bus lines and one of the common electrode lines.

During an inspection mode, in order to easily specify a defective location, a plurality of address marks are provided for the gate bus lines (the common electrode lines) and the signal bus lines (see JP-A-2000-147549). This will be explained later in detail.

In the above-described prior art LCD apparatus, however, there are the following problems. First, when a static charge is transferred by means of a spark or the like to one address mark, since the address mark is electrically isolated, the static charge is consumed as Joule heat therein, so that the address mark is melted, which would generate defects by dust. Second, if each of the address marks serves as a test pad so that the address marks are exposed to the air, when a rubbing process using a rubbing roller is performed upon the address marks, the address marks are peeled off, which also would generate defects by dust.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an LCD

apparatus with address marks capable of avoiding defects by dust.

According to the present invention, in an LCD apparatus including a transparent substrate, a plurality of first bus lines formed on the transparent substrate, a plurality of second bus lines formed on the transparent substrate substantially perpendicular to the first bus lines, a plurality of common electrode lines formed on the transparent substrate in parallel with the first bus lines, and a plurality of pixels each connected to one of the first bus lines, one of the second bus lines and one of the common electrode lines, a plurality of address marks are formed on the transparent substrate and each of the address marks is connected to one of the first bus lines, the second bus lines and the common electrode lines. Thus, since each of the address marks is connected to one of the bus lines and the common electrode lines, even if a static charge is transferred to one of the address marks, the static charge is transferred to the bus lines or the common electrode lines, which would avoid defects by dust.

Also, the address marks are covered by an insulating layer. Thus, even if a rubbing process is performed upon the address marks, the address marks are hardly peeled off, which also would avoid defects by dust.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description set forth below, as compared with the prior art, with reference to the accompanying drawings, wherein:

Fig. 1 is a plan view illustrating a prior art LCD apparatus;

Fig. 2 is a partial circuit diagram of the LCD apparatus of Fig. 1;

Fig. 3 is a plan view of the address marks of Fig. 2;

Fig. 4 is a cross-sectional view taken along the line IV-IV of Fig. 3;

Fig. 5 is a plan view for explaining a problem in the address marks of Fig. 3;

Fig. 6 is a cross-sectional view for explaining another problem in the address marks of Fig. 3;

Fig. 7 is a plan view illustrating a first embodiment of the LCD apparatus according to the present invention;

Fig. 8 is a cross-sectional view taken along the line VIII-VIII of Fig. 7;

Fig. 9 is a plan view for explaining an effect in the address marks of Fig. 7;

Fig. 10 is a cross-sectional view for explaining another effect in the address marks of Fig. 7; and

Fig. 11 is a plan view illustrating a second embodiment of the LCD apparatus according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the preferred embodiments, a prior art LCD apparatus will be explained with reference to Figs. 1, 2, 3, 4, 5 and 6.

In Fig. 1, which is a plan view illustrating a prior art LCD apparatus, a gate bus line GL_i (i=1, 2, ···, m) and a signal bus lines SL_j (j=1, 2, ···, n) are provided on a transparent substrate 17, and a pixel P_{ij} is provided at an intersection between the gate bus line GL_i and the signal bus line SL_j. Also, the pixel P_{ij} is constructed by a thin film transistor (TFT) Q, a liquid crystal cell LC and a storage capacitor SC. In this case, the liquid crystal cell LC is connected to a common electrode line CE_j arranged in parallel with the gate bus line GL_i. Also, the storage capacitor SC is connected to an adjacent gate line in a gate storage type or a storage line (not shown) in a storage capacitor type, thereby substantially increasing the capacitance of the liquid crystal cell LC.

Also, gate (scan) terminals 12 are provided on the transparent substrate 11 and one of the scan terminals 12 is connected to the gate bus line GL_i. Similarly, signal terminals 13 are provided on the transparent substrate 11 and one of the signal terminals 13 is connected to the signal bus line SL_j.

Further, common terminals 14 and terminal blocks 15 are provided and are connected to the common electrode line CE_i. The common electrode line CE_i is connected to two main common

electrode lines CE0 and CE0' which are connected via the terminal blocks 15 to the common terminals 14. Note that Fig. 2 illustrates a partial circuit diagram of the LCD apparatus of Fig. 1 around the main common electrode line CE0.

In the LCD apparatus of Fig. 1 and 2, in order to easily specify a defective location, an address mark is provided for the gate bus line GL_i and the common electrode line CE_i (i=1, 2, ···, m) as illustrated in Fig. 3 (see Fig. 3 of JP-A-2000-147549). For example, a scan address mark "617" is provided for the gate bus line GL_{617} and the common electrode line CE_{617}, and a scan address mark "618" is provided for the gate bus line GL_{618} and the common electrode line CE_{618}.

As illustrated in Fig. 4, the address marks "617", "618", ··· are made of the same material of the common electrode lines CE_i (i=1, 2, ···, m). For example, this material is Cr, Al or Mo. In this case, if each of the address marks serves as a test pad, although the gate bus line GL_i and the common electrode line CE_i are covered by an insulating layer 16 made of silicon oxide or silicon nitride, the address marks are exposed to the air.

The address marks of Figs. 3 and 4 have the following problems. First, as illustrated in Fig. 5, when a static charge +q is transferred by means of a spark or the like to one address mark, the static charge +q is consumed as Joule heat therein, so that the address mark is melted, which would generate defects by dust. Second, if each of the address marks serves as a test pad so that the address marks are exposed to the air, as illustrated in Fig. 6, when a rubbing process using a rubbing roler 17 is performed upon the address marks, the address marks are peeled off, which also would generate defects by dust.

In Fig. 7, which illustrates a first embodiment of the LCD apparatus according to the present invention, an address marks provided for the gate bus line GL_i and the common electrode line CE_i(i=1, 2, ···, m) is connected to the common electrode line CE_i(i=1, 2, ···, m). For example, a scan address mark "617" is connected to the common electrode line CE_{617}, and a scan address mark "618" is

connected to the common electrode line CE_{618}.

As illustrated in Fig. 8, the address marks "617", "618", ··· are made of the same material as the common electrode lines CE_i (i=1, 2, ···, m). For example, this material is Cr, Al or Mo. In this case, the address marks as well as the gate bus line GL_i and the common electrode line CE_i are covered by an insulating layer 16 made of silicon oxide or silicon nitride, so that the address marks are not exposed to the air.

The address marks of Figs. 7 and 8 have the following effects. First, as illustrated in Fig. 9, when a static charge +q is transferred by means of a spark or the like to one address mark, the static charge +q is transferred to the common electrode line CE_{617}, so that the address mark is not melted, which would not generate defects by dust. Second, since the address marks are not exposed to the air, as illustrated in Fig. 10, when a rubbing process using a rubbing roller 17 is carried out, the address marks are hardly peeled off due to the presence of the insulating layer 17, which would not generate defects by dust.

In Fig. 11, which illustrates a second embodiment of the LCD apparatus according to the present invention, an address mark provided for the gate bus line GL_i and the common electrode line CE_i(i=1, 2, ···, m) is connected to the gate bus line GL_i(i=1, 2, ···, m). For example, a scan address mark "617" is connected to the gate bus line GL_{617}, and a scan address mark "618" is connected to the gate bus line GE_{618}.

In the second embodiment, the same effects as in the first embodiment can be expected.

In the above-described embodiments, although one address mark is provided for the gate bus line GL_i and the common electrode line CE_i, one address mark can be provided for the signal bus line SL_j.

Also in the above-described embodiments, although the address marks are constructed by numerals, the address marks can be constructed by letters or combinations of numerals and letters.

As explained hereinabove, according to the present

invention, defects by dust can be avoided.